REMARKS

This paper is responsive to the Final Office Action dated November 4, 2005. Applicant has not amended any of the claims. Claims 1, 7-13, 15, 19-20, 23, 25, and 27 remain pending.

In the Final Office Action, the Examiner rejected claims 1, 7-10, 12-13, 15, 23, 25 and 27 under 35 U.S.C. 102(b) as being anticipated by Kaneko (JP2002084930 or US 2003/0221066); and rejected claims 11, 19 and 20 under 35 U.S.C. 103(a) as being unpatentable over Kaneko in view of Jones et al. (US 6,438,638). Applicant respectfully traverses the rejections.

As a preliminary matter, Applicant notes that Kaneko does not appear to qualify as prior art under 35 U.S.C. 102(b), although it may qualify under 35 U.S.C. 102(e). Applicant reserves the right to challenge the prior art status of this reference, and also reserves the right to demonstrate prior invention. However, given the differences between Kaneko and Applicant's claims, addressed below, the prior art status of Kaneko should be a moot point.

The memory card architecture specifically recited by Applicant's claims is fundamentally different than that taught by Kaneko. For this reason, the rejections under 35 U.S.C. 102 and 35 U.S.C. 103 are improper and must be withdrawn. Moreover, Jones provides no teaching that would remedy the deficiencies of Kaneko with respect to the independent claims. In view of the following remarks, Applicant believes that all pending claims should be allowed over the prior art of record.

Applicant's pending claims recite a memory card that includes two different connectors. In particular, all pending claims require that the memory card include a first connector that conforms to a first connector standard and a second connector that conforms to a second connector standard. Claims 1 and 15 are independent claims directed to memory cards. Claims 23 and 27 are independent claims directed to systems that include a memory card and the first and second devices to which the memory card can be attached via the first and second connectors. The memory card recited in claim 1 is similar to that recited in system claim 23, while the memory card recited in claim 15 is similar to that recited in new system claim 27. All of these claims also require that the first connector standard comprises a host computer connector (HCC) standard and the second connector standard comprises a device communication connector (DCC) standard.

As noted by the Examiner, Kaneko teaches a memory card that includes two different connectors. For purposes of this abbreviated "After-Final" response, Applicant does not dispute the Examiner's conclusions that Kaneko discloses a first connector that complies with a host computer connector (HCC) standard and a second connector that complies with a device communication connector (DCC) standard, as required by all pending claims.

However, the memory card of Kaneko is fundamentally different than those recited in Applicant's claims in another respect. In particular, Applicant's claims recite a different controller architecture than that of Kaneko. Kaneko lacks any suggestion, whatsoever, of the controller architecture required by Applicant's different claims.

More specifically, claims 1 and 23 require that the memory card includes *a controller that controls the memory and controls output via the first connector and the second connector*. In stark contrast to this requirement of claims 1 and 23, Kaneko discloses a less efficient architecture that includes three different controllers. In particular, Kaneko discloses one controller for the memory, one for the first connector, and one for the second connector. None of the controllers of Kaneko, however, controls both the memory and output via the connectors, as required by claims 1 and 23.

Claims 15 and 27 require that the memory card include two controllers, i.e., first and second controllers. The first controller is electrically coupled to the memory and the first connector, and *controls both the memory and output via the first connector*. The second controller is electrically coupled to the second connector and the first controller, and the second controller controls output via the second connector.

Thus, claims 15 and 27 require two controllers, but one of the controllers controls both the memory and output via one of the connectors. This clearly distinguishes the claimed invention from Kaneko, which again, requires three different controllers for the memory, the first connector and the second connector, respectively. None of the controllers of Kaneko controls both the memory and output via a connector.

Applicant also respectively notes that the Examiner's analysis appears to overlook the different requirements of claims 15 and 27 relative to the requirements of claims 1 and 23. Indeed, the Examiner grouped all of claims 1, 15, 23 and 27 together in the analysis of the Final Office Action, notwithstanding the differences between claims 15 and 27 relative to claims 1 and

23. Thus, it appears that the Examiner may have overlooked the differences between claims 1 and 23 and Kaneko, as well as the differences between claims 15 and 27 and Kaneko.

In order to support an anticipation rejection under 35 U.S.C. 102, it is well established that a prior art reference must disclose each and every element of a claim. This well known rule of law is commonly referred to as the "all-elements rule."[1] If a prior art reference fails to disclose any element of a claim, then rejection under 35 U.S.C. 102 is improper. [2]

In this case, Kaneko does not disclose or suggest *a controller that controls the memory and controls output via the first connector and the second connector*, as required by claims 1 and 23. Furthermore, Kaneko does not disclose or suggest *a controller that controls both the memory and output via one of two different connectors*, as required by claims 15 and 27. In the context of a memory card that includes two different connectors (as also required by Applicant's claims), the two different controller architectures recited in the different claims, as discussed above, is novel and non-obvious over the applied prior art.

In view of the fundamental distinctions outlined above, all pending rejections are improper and must be withdrawn. The Jones reference provides no teaching that would remedy the deficiencies of Kaneko with respect to the independent claims. Therefore, Applicant reserves further comment on the Jones reference at this time.

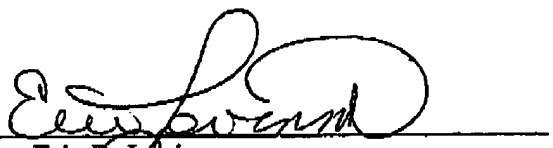
---

[1] *See Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81 (CAFC 1986) ("it is axiomatic that for prior art to anticipate under 102 it has to meet every element of the claimed invention").
[2] *Id. See also Lewmar Marine, Inc. v. Barient, Inc.* 827 F.2d 744, 3 USPQ2d 1766 (CAFC 1987); *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (CAFC 1990); *C.R. Bard, Inc. v. MP Systems, Inc.*, 157 F.3d 1340, 48 USPQ2d 1225 (CAFC 1998); *Oney v. Ratliff*, 182 F.3d 893, 51 USPQ2d 1697 (CAFC 1999); *Apple Computer, Inc. v. Articulate Systems, Inc.*, 234 F.3d 14, 57 USPQ2d 1057 (CAFC 2000).

Application Number 10/644,484
After-Final Response to Final Office Action mailed November 4, 2005

All claims in this application are in condition for allowance. Applicant respectfully requests reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 09-0069. The Examiner is invited to telephone the below-signed attorney to discuss this application.

Date: 12/21/5

By: 

Name: Eric D. Levinson
Reg. No.: 35,814

Imation Legal Affairs
P.O. Box 64898
St. Paul, Minnesota 55164-0898
Telephone: (651) 704-3604
Facsimile: (651) 704-5951